Notice of Allowability	Application No.	Applicant(s)	
	09/580,854	SIRICHOTIYAKUL ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *27 July 2005*.

2. ☒ The allowed claim(s) is/are *1-29 and 31-44*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated July 27, 2005. Claims 1-29 and 31-44 of the application are pending.

Drawings

2. The drawings submitted on May 30, 2000 are accepted.

Examiner's Amendment

3. Authorization for this examiner's amendment was given in a telephone conversation by Ms. Joanna G. Chiu on September 20, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. In the claims:

Claim 32, Line 7, "calculating a leakage for each transistor in a second set of transistors"

has been changed to

-- calculating a leakage current for each transistor in a second set of transistors --.

Claim 41, Lines 1-2, "A program stored on a computer readable medium, that includes a plurality of computer executable instructions, the program comprising:"

has been changed to

-- A program stored on a computer readable medium including a plurality of computer executable instructions which when executed on a computer performs a process for determining a dominant logic state in an integrated circuit, the program comprising:--.

Claim 42, Lines 1-2, "A program stored on a computer readable medium, that includes a plurality of computer executable instructions, the program comprising:"

has been changed to

-- A program stored on a computer readable medium including a plurality of computer executable instructions which when executed on a computer performs a process for determining a leakage current of an integrated circuit, the program comprising:--.

Claim 43, Lines 1-3, "A computer readable medium having stored therein a program comprising instructions which when executed on a computer perform a process for analyzing an integrated circuit"

has been changed to

-- A computer readable medium having stored therein a program comprising instructions which when executed on a computer perform a process for improving performance of an integrated circuit --.

Claim 43, Lines 17-18, "a fourth plurality of instructions for determining a cone of influence of the selected one of the transistors"

has been changed to

-- a fourth plurality of instructions for modifying an area of at least one transistor within the integrated circuit --.

Claim 44, Lines 1-2, "A program stored on a computer readable medium, that includes a plurality of computer executable instructions, the program comprising:"

has been changed to

-- A program stored on a computer readable medium including a plurality of computer executable instructions which when executed on a computer performs a process for calculating a leakage current of an integrated circuit, the program comprising:--.

Claim 44, Lines 9-10, "a fourth plurality of instructions for calculating a leakage for each transistor in a second set of transistors"

has been changed to

-- a fourth plurality of instructions for calculating a leakage current for each transistor in a second set of transistors --.

Reasons for Allowance

5. Claims 1-29 and 31-44 of the application are allowed over prior art of record.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a method of selecting device threshold voltages in optimizing circuit design for high speed and low power consumption; transistors with low threshold voltage operate at higher speeds but increase leakage current and static power consumption; the critical paths in which the delay between circuit elements exceeds the maximum timing constraints are identified; certain transistors on the critical path are selected according to their propensity to increase speed while minimizing static power consumption, and their threshold voltage lowered; the circuit is then simulated and if the circuit fails to meet the timing constraints, additional transistors in the path are assigned lower threshold voltage (**Reyes et al.,** U.S. Patent 5,774,367);

(2) a system and method for selecting sizes of components for integrated circuits; the method chooses initial sizes of the transistors to obtain desired performance of the circuit; the timing is verified using computer based tools; then one or more object are selected for resizing; the cones of objects influenced by a change in selected objects are identified; for each selected object and each object in the cones of influence, new size is calculated; a timing simulator is

used to develop the performance profile of area vs power vs delay for the circuit (**Gristede et al.,** U.S. Patent 6,175,949); and

(3) a method of reducing power consumption in circuits; the method identifies the excessive power consuming sites; the excessive power consuming site is monitored for an indeterminate logic state which results in leakage current and excessive power consumption; the locations of the leakage current sites are identified and the circuit design modified (**Horr et al.,** U.S. Patent 5,515,302).

None of these references taken either alone or in combination with the prior art of record discloses a computer implemented method for determining a dominant logic state in an integrated circuit, specifically including:

"using a representation of the integrated circuit to determine a first partition and a second partition wherein the first partition includes a first power supply node and the second partition includes a second power supply node;

determining a partial logic state corresponding to the first and second partitions;

modifying the representation according to the partial logic state; and

using the modified representation to determine the dominant logic state".

None of these references taken either alone or in combination with the prior art of record discloses a computer implemented method for determining a leakage current of an integrated circuit, specifically including:

"determining a dominant logic state corresponding to the at least one DCC; and

calculating a leakage current for the at least one DCC corresponding to the dominant logic state".

None of these references taken either alone or in combination with the prior art of record discloses a computer implemented method of improving performance of an integrated circuit, specifically including:

"partitioning the integrated circuit into at least one DC-connected component (DCC);

determining a dominant logic state corresponding to the at least one DCC; and

calculating a leakage current for the at least one DCC corresponding to the dominant logic state".

None of these references taken either alone or in combination with the prior art of record discloses a computer implemented method for calculating a leakage current of an integrated circuit, specifically including:

"constructing a graph having nodes and edges according to a dominant logic state of the integrated circuit;

calculating a leakage current for each transistor in a first set of transistors".

None of these references taken either alone or in combination with the prior art of record discloses a program stored on a computer readable medium including a plurality of computer executable instructions for determining a dominant logic state in an integrated circuit, specifically including:

"a second plurality of instructions for determining a first partition and a second partition wherein the first partition includes a first power supply node and the second partition includes a second power supply node;

a third plurality of instructions for determining a partial logic state corresponding to the first and second partitions;

a fourth plurality of instructions for modifying the representation according to the partial logic state; and

a fifth plurality of instructions for using the modified representation to determine the dominant logic state".

None of these references taken either alone or in combination with the prior art of record discloses a program stored on a computer readable medium including a plurality of computer executable instructions for determining a leakage current of an integrated circuit, specifically including:

"a second plurality of instructions for determining a dominant logic state corresponding to the at least one DCC; and

a third plurality of instructions for calculating a leakage current for the at least one DCC corresponding to the dominant logic state".

None of these references taken either alone or in combination with the prior art of record discloses a computer readable medium having stored therein a program comprising instructions for improving performance of an integrated circuit, specifically including:

"partitioning the integrated circuit into at least one DC-connected component (DCC);

determining a dominant logic state corresponding to the at least one DCC; and

calculating a leakage current for the at least one DCC corresponding to the dominant logic state".

None of these references taken either alone or in combination with the prior art of record discloses a program stored on a computer readable medium including a plurality of computer executable instructions for calculating a leakage current of an integrated circuit, specifically including:

"a first plurality of instructions for receiving a graph having nodes and edges according to a dominant logic state of an integrated circuit;

a second plurality of instructions for calculating a leakage current for each transistor in a first set of transistors".

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Paul L. Rodriguez 9/21/05
Primary Examiner
Art Unit 2125

K. Thangavelu
Art Unit 2123
September 20, 2005